

METHOD AND A DEVICE FOR TESTING ELECTRONIC MEMORY DEVICES

TECHNICAL FIELD

This invention relates to a method of testing electronic memory devices. The invention also concerns a control device implementing the inventive method.

5 BACKGROUND OF THE INVENTION

As is well known, a prominent feature of electronic non-volatile memory devices, *e.g.*, last-generation flash memory devices, is that a control logic circuit portion is incorporated in them to form an integral part the device. The control logic is not of inconsiderable complexity and importance being, as it is, requisite for executing program and erase algorithms.

The control logic circuit portion may be provided in different forms, such as any of those listed here below.

1. A wired logic, wherein the sequence of the functions to be performed is implemented by a network purely of logic gates. Understandably, in the event of modifications occurring in the instruction flow as a result of design alterations or changed technological requirements, the logic circuit portion must be entirely redesigned.

2. A finite state machine, consisting essentially of either a Moore's or a Mealey's machine the combinational portion whereof is provided by a PLA (Programmable Logic Array) logic structure. In the event of modifications being made, it suffices that the PLA logic structure be reprogrammed, for example by changing a limited number of masks, to implement a new function. In this case, the overall circuit design would be retained, to the benefit of modification and simulation times and cost of the operation.

3. A microprogrammed unit, which contains an instruction algorithm in a memory array. The instructions are carried out by a sequencer which is identical with those provided in microcontrollers and microprocessors. The algorithm-storing memory array may be any non-volatile memory, *e.g.*, a ROM, in which case reprogramming will

entail modifications to some masks, a PROM, EPROM, EEPROM, or flash-type memory, in which case reprogramming may be software based.

Additionally to executing user's algorithms, the control logic is used:

at the characterizing stage, to check all the logic and analog parts for full operability by emulating the user-mode operation to be, or measuring such characteristic parameters as the value attained by voltage boosters, if provided, or the value of the internally generated reference voltage.

at the EWS (Electrical Wafer Test) or final test stage, to perform all those operations that will make the memory ready for use by the ultimate customer, such as reference cell writing, setting up special UPROM or OTP registers, etc..

It will be appreciated from the foregoing that the control logic circuit portion exacts careful designing, not only on account of its complex structure but also, and above all, of the need to have the operability of its many functions thoroughly checked. Incomplete coverage of all its operational aspects, and consequent circuit malfunctions, would require corrective actions which are specific to the type of the implementation used.

Wired logic-based approaches apparently admit of no corrective action.

Approaches based on a finite-state machine or a microprogrammed unit do admit of reprogramming, with greater or lesser degrees of difficulty. In all cases, however, the memory device must be tested before full operability of the control logic can be ascertained.

To test the control logic for its operability, techniques known as DFT (Design For Testability) are usually resorted to. These techniques consist of using special sequences or chains of storage components, *e.g.*, latches and/or flip-flops, having a load input and an output for cascade connection to the next component in the chain. In the test mode, these "test chains" are loaded with predetermined data sequences as if they were single serial registers. Briefly, the control logic incorporates a hardware portion specially for performing test operations.

In response to forcing said data sequence, the control logic provides something of a "reaction to stimulus", and a record of the data sequences and their

responses, when compared with expected results provided by a simulation, will allow conformity of the circuit with the specifications to be verified and guaranteed. A drawback with the above testing method is that complex gates must be included in the design of the control logic portion devoted to testing, which expands the area requirements of the device to a considerable extent.

A commonly adopted solution consists of testing only the analog circuitry, and is followed by characterization. Where the operability of the various parts of the control logic are to be tested in situations other than those provided for by the algorithm, a certain number of test registers are included which are effective to drive the analog circuits, once suitably loaded. Again, the overall area for occupation by the circuit must be expanded, merely to enable the testing operations to be performed.

The technical problem underlying this invention is to provide a method of testing integrated memory devices with features appropriate to allow plural testing operations to be carried out, while avoiding the need for the circuit under test to incorporate dedicated circuit portions merely to enable such operations to be performed.

SUMMARY OF THE INVENTION

The principle on which this invention stands is that of having an external programmable control logic, detachably connected to the memory device, temporarily used instead of the resident control logic.

Based on this principle, the technical problem is solved by a testing method as previously indicated wherein it comprises temporarily using a test operation control device for said control logic, which test operation control device is external of and connected detachably to the memory device.

The invention also relates to a control device for use in testing electronic memory devices provided with a matrix array of memory cells and a control logic circuit portion associated with the memory cell array, as well as with circuitry associated with said control logic, wherein it comprises a memory unit external to the control logic.

The features and advantages of the method and the device according to this invention will be apparent from the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawing.

In the drawing:

5 BRIEF DESCRIPTION OF THE DRAWING

The one Figure shows schematically an electronic memory device as associated with a testing device embodying this invention.

DETAILED DESCRIPTION OF THE INVENTION

With reference to the drawing Figure, an electronic memory device,
10 preferably of the semiconductor integrated type, is generally shown at 1 in schematic form.

This memory device 1 may be a non-volatile memory, *e.g.*, a PROM, EPROM, EEPROM, or flash EPROM. However, it would be possible for this memory to be a volatile memory.

The memory device 1 comprises a matrix array 2 of non-volatile memory
15 cells, and associated circuitry 3. The memory device 1 further comprises a control logic circuit portion 4 which is two-way connected to the array 2 by an internal bus 5. The control logic 4 is two-way connected to the circuitry 3 as well.

Advantageously in this invention, a test operation control device 9 is
20 associated temporarily with the memory device 1 by detachable connection to the memory device 1.

More particularly, the control device 1 may be an external memory array 7, *e.g.*, of the non-volatile type, substantially like that incorporated in the device 1. In another embodiment, the control device 9 may be a control logic substantially like that incorporated in the device 1.

25 The detachable connection between the test operation control device 9 and the memory device 1 is established, using data input/output pins 6 along with address and control signal input pins 8, over respective connection buses 11 and 10.

It is through these pins 6, 8 and buses 11, 10, that the control device 9 is temporarily two-way connected to the control logic 4 of the memory 1.

The invention proceeds from the consideration that a control logic unit 4 already is included in the memory device 1 and operative, for the purposes of the user's algorithms, to control all the other circuit portions of the memory 1 by an appropriate algorithm.

The solution to the problem resides in temporarily "replacing" the cell array 2 with another array 7, external of the device 1, Which is one example of, or a portion of the test operation control device 7, as shown in the drawing. According to the principles of the invention the external array 7 is used to simulate the internal memory 2, making possible the direct test and observation of the interaction of the control logic 4 with the array 7. The external memory array 7 can be an actual hardware memory, identical to the internal memory array 2. Alternatively, it may be a simulated array, having some portions in hardware and some in software, or all portions in software, to simulate the relevant portions and operations of the internal memory array 2. As will be appreciated, the test operation control device 9 may also comprise logic circuitry to simulate the control logic 4, for the purpose of testing and observing the memory array 2 directly, and in isolation from the control logic.

Thus, the invention is advantageous especially in that it allows the control algorithm of circuit portions of the memory device 1 to be changed in order to carry out a series of different tests. This not only allows the circuit portions of the device 1 to be controlled as desired, but also the control logic 4 itself to be isolated and tested for operability in a self-diagnosis mode.

These are not features that a conventional microprogrammed unit can possibly offer, because its code-storing array would be substantially unchangeable unless masks are changed, where ROMs are involved, or the contents is altered, where flash memories are involved. Also, any alterations would take a long time to check the operation for its effectiveness.

Where a test program is to be run instead of the standard one, the method of this invention provides for the control logic 4 to read from the external memory rather than from the internal array 2. The input/output pins of the device 1 can be utilized for the purpose.

5 For example, the address of the external memory 7 (*i.e.*, the program counter) can be supplied through the data pins 6, while through the address pins 8, the external memory 7 will supply the internal logic with an instruction for decodification and execution by it.

The test procedure can be controlled using any combinations of control or
10 address signals (CE, WE, addresses and/or data not involved in the above loop, etc.).

With the method of this invention, debugging time can be improved, at the same time as the algorithms used in the memory device are optimized. The algorithms of today's multi-level flash memories are highly complicated (450-minterm PLA), and written in hardware format.

15 Upon the memory device leaving the production lines, the above algorithms are run with a considerable expenditure of effort by the person in charge of the debugging operations.

Although the program memory is resident in the memory device 1, this invention allows it to be bypassed, and a faster analysis of the whole device performed.

20 The method and device of this invention do solve the technical problem and offer a number of advantages, as specified here below.

Testing the various parts of the device can be made flexible for no added complexity and area requirements. A multiplexer and an identification protocol may be used, if desired, for a command to "substitute".

25 At the initial stage (EWS and Final Test) of characterizing the memory device, the algorithm flow can be altered at will, and an optimum solution found with no need for expensive hardware modifications.

The operability of the control logic can be tested *per se*.

The operability of (analog, matrix, etc.) circuits usually utilized by the above logic in the user mode can be likewise tested.

A different algorithm from that actually “written” in the PLA or the ROM of the microprogrammed unit may be implemented merely for testing purposes,
5 without altering its contents.

In the light of the foregoing, changes and modifications may be made unto the method and the device of this invention by a skilled person in the art, still within the scope of the following claims.